What is claimed is:

1. A semiconductor integrated circuit device comprising:

a first semiconductor chip having a nonvolatile memory for storing redundancy information; and

a second semiconductor chip having a conversion circuit for converting the redundancy information output in a form of serial data from the nonvolatile memory into parallel data and a redundancy circuit of which an output state is definitely set by receiving the parallel data output from the conversion circuit.

2. A semiconductor integrated circuit device as claimed in claim 1,

wherein the nonvolatile memory and the conversion circuit are connected together by way of a bump.

3. A semiconductor integrated circuit device as claimed in claim 1,

wherein the second semiconductor chip further has a redundancy data loading control circuit that feeds the nonvolatile memory with operation commands and that controls operation of the conversion circuit.

4. A semiconductor integrated circuit device as claimed in claim 3,

wherein the nonvolatile memory and the conversion circuit are connected together by way of a bump, and

the nonvolatile memory and the redundancy data loading control circuit are connected together by way of a bump

5. A semiconductor integrated circuit device as claimed in claim 1, wherein the second semiconductor chip has conductors laid in multiple layers.

6. A semiconductor integrated circuit device as claimed in claim 2, wherein the second semiconductor chip has conductors laid in multiple layers.

7. A semiconductor integrated circuit device as claimed in claim 3, wherein the second semiconductor chip has conductors laid in multiple layers.

8. A semiconductor integrated circuit device as claimed in claim 4, wherein the second semiconductor chip has conductors laid in multiple layers.